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**Project Partners**



**Background and Objectives:**

In the coming Internet of Things (IoT) Era, within the next few years 20 to 50 billion devices are expected to be wirelessly connected and to communicate intelligently to each other in real time providing the most up-to-date information. To further enable wide scale deployment of sensors with proven low power operation and highly reliable time-synchronized performance a new innovative design and technology solutions will be required.

The IoT devices cover a wide range of devices and application. They will have different characteristics, functionality and power level, memory requirements, computing resources, costs and thus technology options. Devices and systems of swarm sensor node with ultra low power and low cost attributes will likely be built on older technology generations, such as 40nm CMOS to enable SoC integration of all system components including RF, memory blocks and sensor data processing. For the systems demanding more computing power at relatively low power consumption more advanced technology nodes will be required, such as 28nm or 22nm CMOS node. FDSOI as low power technology will allow high performance computing with low power consumption and enable new IoT devices partly powered by mobile energy sources.

**Approach:**

The goal of the PRIME project is to establish an open Ultra Low Power (ULP) Technology Platform containing all necessary design and architecture blocks and components which could enable the European industry to increase and strengthen their competitive and leading eco-system and benefit from market opportunities created by the Internet of Things (IoT) revolution.

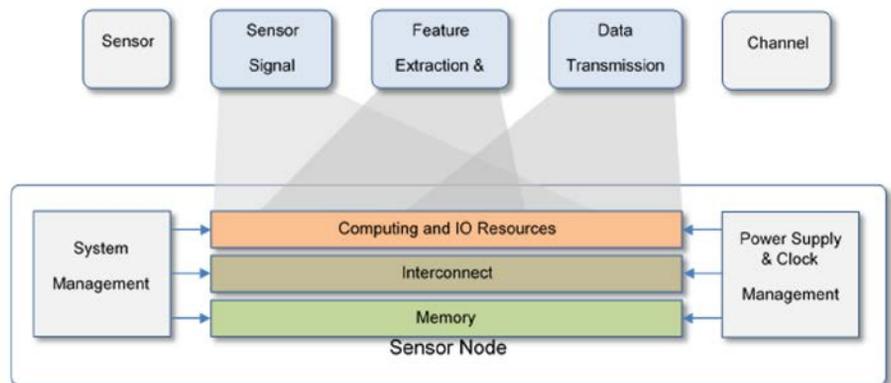
Over 3 years the project will develop and demonstrate the key building blocks of IoT ULP systems driven by the applications in the medical, agricultural, domestics and security domains. This will include development of high

performance, energy efficient and cost effective technology platform, flexible design ecosystem (including IP and design flow), changes in architectural and power management to reduced energy consumption, security blocks based on PUF and finally the System of Chip and System in Package memory banks and processing implementations for IoT sensor node systems.

Developed advanced as 22nm FDSOI low power technologies with logic, analog, RF and embedded new memory components (STT RAM and RRAM) together with innovative design and system architecture solutions will be used to build macros and demonstrate functionality and power reduction advantage of the new IoT device components. The PRIME project will realize several demonstrators of IoT system building blocks to show the proposed low power wireless solutions, functionality and performance of delivered design and technology blocks. The consortium semiconductor ecosystem (IDMs, design houses, R&D, tools & wafer suppliers, foundries, system/product providers) covers complementarily all desired areas of expertise to achieve the project goals.

**Vodafone Chair Contribution:**

The Vodafone Chair's scientific and technical contributions will be the development of hardware components for an efficient power management and data transmission as well as digital data processing and memory units in an heterogeneous MPSoC architecture. In collaboration with the TUD's Chair of Highly-Parallel VLSI-Systems and Neuro-Microelectronics, the components will be integrated into an MPSoC suitable for fabrication in 22nm FDSOI technology. For interconnecting the hardware components, a Network on Chip (NoC) will be designed to handle complex data. In the end, a demonstrator platform will be set up. Besides that, the Vodafone Chair will take part in the dissemination activities by presenting the project results in major conferences and journals, respectively.



PRIME principle of node functionality and system mapping