Venturing Electronics into Unknown Grounds

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***Abstract*—Electronics is a huge driver for economic success of today's societies. cfaed, the German Cluster of Excellence located in Dresden (Germany), aims at pushing the boundaries of electronics into unknown grounds. This includes not only current electronics but also scientist's and engineer's projection of how the electronics landscape will look like in the future. We pursue an approach that connects all layers from new materials to new system design (vertical) as well as across our Research Routes (horizontal) and ensure coherence through adequate measures. cfaed is centered at one location which, combined with our unique approach, places it above the highly funded Competitive Landscape.**

I. Introduction / Main Research Objective

Electronics is a crucial driver for innovation in modern societies. It is the basis for finding solutions to big societal problems. The innovation in electronics thrives on delivering ever-increasing capabilities that fuel and drive the success of many applications, e.g., wireless communications, machine learning, Industry 4.0, Internet of Things, and the Tactile Internet.

In traditional CMOS, Moore's law, i.e. doubling of the number of transistors per chip every 18 months, has been a good estimate for what to expect. However, as CMOS technology is reaching atomic boundaries, Moore's law is projected to end and new ways must be explored to enable continued innovation. In particular, innovating electronics requires addressing the following challenges: small physical size, speed, energy efficiency, new functionality, self-assembly/-organization, adaptivity, resilience and low cost.

Accurately estimating the performance of future electronics is so crucial that both industry and science communities identified the need to map the potential of its future, leading to the creation of the ITRS and, since 2016, the IRDS roadmap (International Technology Roadmap for Semiconductors/International Roadmap for Devices and Systems, https://irds.ieee.org). It not only outlines the potential of electronics innovation, but also points out the boundaries of what seems achievable based on current knowledge. With valuable insights gained within cfaed's current funding period (hereafter referred to as cfaed-1[1]), we are convinced that we can generate breakthroughs that push some of the IRDS boundaries, enabling continued innovation in the coming funding period (cfaed-2).

Among many other smaller scientific and structural goals, cfaed's main research objective and vision is to **generate breakthroughs in electronics showing a path beyond current roadmaps**. This cannot be done by extending and optimizing existing ideas but only through exploiting radically new scientific discoveries.

Hence, an interesting research challenge arises. Can electronics be driven beyond the currently known boundaries, and if yes, what is an approach to do this? On the US side, DARPA has come to realize this untapped research ground, and rolled out the heavily funded ($216 Mio.) Electronics Resurgence Initiative (ERI) in 2017 [1]. Within the last 6 years, cfaed has started addressing this interesting research topic, and has come to the conclusion that we should be able to advance electronics "into unknown grounds".

This paper sketches cfaed's research approach and work program. In section II, the *research approach* is presented, i.e. we address the question: *How does cfaed plan to reach its main objective?* In section III, the Research Program of cfaed is presented. In section IV, cfaed's horizontal measures, which are put in place to ensure research coherence, are outlined. Finally, section V concludes the paper.

II. Research Approach

A. Vertical bridging of layers

cfaed has close to seven years of experience in carrying out inspiring collaborative research, where natural & material scientists jointly work with engineering scientists to generate impactful research results, targeted at showing a path for innovation. We learnt that a comprehensive approach, integrating research competency across layers from materials to systems (cf.

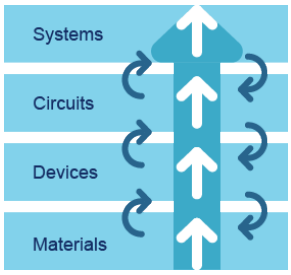

Fig. 1. Multi-layer research approach - bridging the gaps between layers is key to cfaed's success.

[1] cfaed-1 has received close to 6 years of funding as a Cluster of Excellence, one of three funding lines of the Excellence Initiative of the German Federal and State Governments, initiated to strengthen Germany's position as an outstanding place for research in the long term and further improve its international competitiveness.

Fig. 1), requires tailored strategies and instruments, which will be an important focus for cfaed.

From Materials to Devices: Some of the recent significant advances in new materials have now reached a point that warrants exploring device fabrication and circuit design to build novel information processing systems for potential future applications. For this, one has to understand not only how to further explore new materials and their properties, but also how to engineer them for a targeted solution, i.e. a new device with absolutely innovative features.

From Devices to Circuits: The full potential of a new device and its benefits can only be unleashed when building circuits out of these devices. On the one hand, the understanding of the full potential of a circuit requires the analysis and measurement of its capabilities, and bridging the gap between devices and circuits. On the other hand, this guides the device design as well as materials research in finding better solutions.

From Circuits to Systems: Finally, the targeted novel electronic circuits need to be evaluated by exploring their potential for building new systems, which requires research reaching all the way to the area of computer engineering. During cfaed-1, we were reassured that crossing the layers is the road to success. Drawing from our experience and achievements, we evolved our structure and concept incorporating ideas from new investigators and emergent areas of research.

From our experience within cfaed-1, we discovered that it is beneficial to focus the research on its innovation potential by introducing vertical design targets with a circuit outcome, "V-Targets", as described below. They serve to show the measurable potential of our research results. Not all V-Targets are hardware demonstrators, as they might also be a simulation/emulation. They serve to generate focus and coherence between all involved team members. Details are given in the Route Descriptions in section III.

B. Research Structure

Each selected Route of cfaed is based on (i) research insights gained by our researchers during cfaed-1, from which we identified a great potential to push the frontiers ("wall") of IRDS beyond its boundaries, (ii) having identified an approach

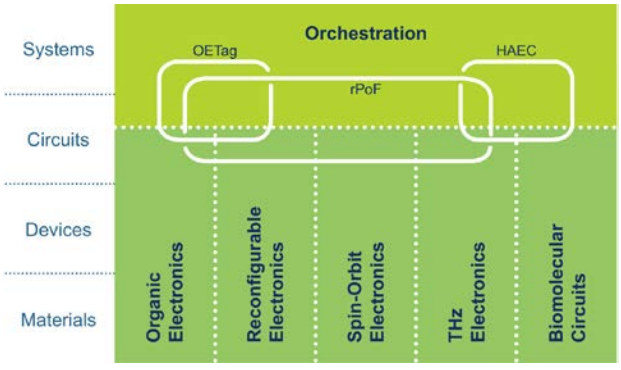

Fig. 2. cfaed's research structure consists of 5+1 Research Routes, linked by Horizontal Integration Targets (HITs)

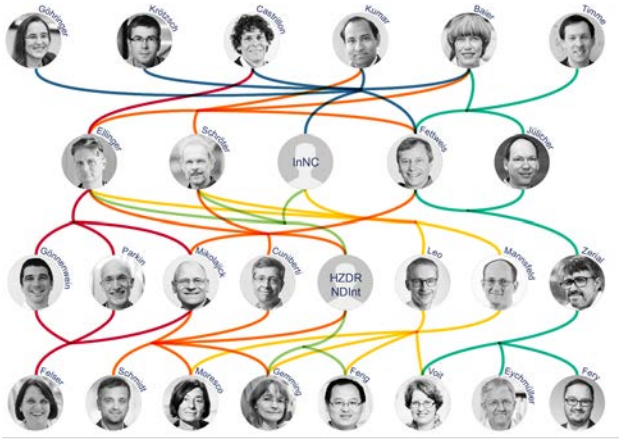

Fig. 3. Multi-layer research approach - bridging the gaps between layers is key to cfaed's success.

to move the "wall", (iii) the right team and favorable environment, and (iv) having identified a measurable benefit for society for advancing electronics.

To optimize our chances, we focus on those research directions that match the four above-mentioned criteria, not withholding others, e.g., quantum computing, which may also possess the potential for advancing electronics beyond IRDS.

This focus led us to establish six Research Routes within cfaed, depicted in Fig. 2. Five Routes envision breakthroughs in enabling new electronics by innovating from materials to circuits. This becomes the basis for the sixth Route to enable new systems.

C. Ensuring Coherence in Research

To foster interplay and coherence between the Routes, as well as to show additional potential when combining the results, we introduce *Horizontal Integration Targets* (HITs). The HITs are crucial for multiple Routes that join forces to achieve common systems goals. They span multiple Routes, as can be seen in Fig. 2. Details on the HITs are given in section IV.

This interplay is facilitated through organizing our research areas into a network of routes which provide the framework for our extensive teamwork in Dresden (see Fig. 3); the scientific achievements obtained in one Route will become applicable to help advance the others, and can be further catalyzed due to the involvement of many investigators active in multiple routes. Our joint research experience has also helped to build a strong team spirit that gives us the adaptability to improve the cluster's structure according to future findings.

In a nutshell, what makes cfaed's approach truly unique is that it firstly, aims at bridging all the involved abstraction layers, starting from materials, devices, circuits, reaching to (information processing) systems, within a new unifying framework and "vertical measures", explained in detail in Section III. cfaed, hence, links a wide range of sciences from material sciences to electrical engineering to computer science. And, secondly, our approach is carried out in multiple research directions by our Routes, which are linked with "horizontal

measures". The combination of the two provides fertile ground for mutual exchange and inspiration.

D. Competitive Landscape

Below, we list important research activities that relate to cfaed as a whole.

USA Here we list just the main activities in the US in the area of cfaed: SRC has funded the STARnet program with DARPA and the NRI program with NSF and NIST until the end of 2017, which cover many aspects of cfaed, however distributed across the US. New SRC initiatives, JUMP co-funded with DARPA and nCORE co-funded with NSF/NIST, have started since 2018, with the same model of a distributed US academic research network. Some examples of large US research initiatives and facilities include: (1) DARPA-funded ERI (09/2017, $216 Mio.) tackling new disruptive materials, integration, circuit design and systems architectures, (2) E3S funded by NSF, tackling energy efficiency, centered in Berkeley and MIT; (3) MIT's NanoStructures Lab, focusing e.g., on nanostructuring, self-assembly, and nano-analysis; (4) E2CDA (energy-efficient computing from devices to architectures) funded by NSF and SRC and an outcome of the OSTP Grand Challenge to achieve energy efficiency by co-optimizing emerging devices and architectures; (5) Stanford SystemX funded by industry members, building energy efficient beyond CMOS circuits; (6) on a smaller scale, NEEDS funded by NSF and SRC, focusing on compact models (Purdue, Berkeley, MIT, Stanford); (7) CMU's NanoFab, also facilitating research around novel devices. While there is some overlap with cfaed's mission, many of the above US centers differ. Furthermore, as most are decentralized, strong structural differences apply. In the field of large-scale processing systems, the University of Berkeley has been very influential.

Japan Large programs are funded under CREST, however, geographically distributed. Among others, silicon nanowires and carbon nanotubes are considered. However, the projects lack a system component and are mainly limited to the materials level.

China The Universities in Beijing (e.g., Tsinghua University, Beijing University), Dalian, Chengdu, and other cities have a special focus on hiring talent in areas covered by cfaed. We shall expect research outcomes to become widely visible soon.

Europe Besides the large institutions IMEC, Leti, Tyndall, large research programs are the EU GRAPHENE Flagship, a large center at the University of Manchester. In Germany, two Centers of Excellence (in Erlangen and Munich) focus on materials and functionalization, though not covering devices and circuits. The very large French nano programs mainly focus on research to execute the IRDS. The Swiss Nano-Tera program is focused on health and environment applications, and is in the ramp-down phase. The Swiss BRIDGE program has a broad focus not overlapping with cfaed. The SiNANO program, with many high-profile members, focuses on nanoelectronic research doing both, "More Moore" and "Beyond Moore", however, scattered all over Europe.

In summary, our main differentiator is:

1. A comprehensive vertically integrated approach, spanning from materials to systems.

Furthermore, we are confident that cfaed uniquely demonstrates the combination of the above with the following six key ingredients:

2. One location, making it easy for researchers to meet, exchange, and collaborate;
3. An internationally recognized excellence in research, attracting the best researchers;
4. The local concentration of R&D expertise, attracting scientists and industry;
5. Experience in innovation and proven record of success, in particular, bridging from basic sciences to creating 60+ start-ups;
6. The "Dresden Spirit" of collaboration and joint research, including open sharing of labs;
7. A team with the ambition to push the boundaries of the IRDS roadmap.

III. Research Program

In this section, we give an outline for each of our six Research Routes, clearly stating the identified walls, our approach to overcome them, the benefit we expect from a solution, our recent success that makes us believe in our approach, the measures applied in the Route to reach our goals, and the answer to the question "Why Dresden?".

A. Organic Electronics Route "OE"

Wall Although with our results from cfaed-1 we are able to produce cutting-edge single devices, we cannot yet produce on-demand printable, low-cost circuits. There reason for this is a lack of processes for circuit-grade device fabrication (throughput and uniformity) and materials, more specifically, insufficient carrier mobility.

Approach In order to successfully and rapidly move towards our V-Target, our research is focused on several key areas; we will investigate new materials with unprecedented performance and novel vertical transistor device principles. These materials and device technologies will be employed in fully integrated devices and complex organic circuits. One part of our materials research also specifically focuses on materials for

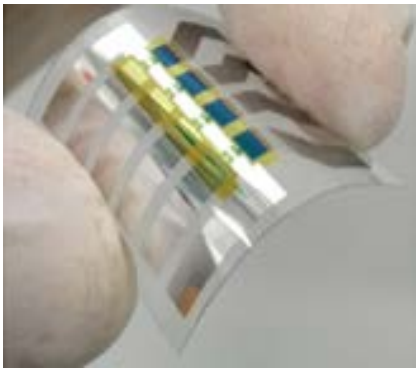

Fig. 2. photograph of a flexible PBT on a PET substrate

printable transistor circuits. We plan to integrate lateral and vertical high-performance OFET devices into circuits in order to combine them with sensors such as our novel near-infrared organic sensors, and to ultimately demonstrate their integration in complex organic devices. We will also employ a new "system-level informed" approach to our research. Instead of developing device technologies without feedback regarding their "real world" (i.e. circuit level) utility, we will develop models and design circuits based on those models that allow us to evaluate our technologies in circuits of a complexity that, while we cannot yet fabricate them, will steer our device and material design. We believe that this approach will allow us to increase the practical impact of Organic Electronics research and to foster closer collaborations with the companies in the Organic Electronics Saxony network, or even kick-start new companies based on our technologies. We will benchmark our best single-device technologies in a far more realistic way than is currently possible.

Benefit Organic Electronics may become the basis for immediately, on-demand manufacturable organic circuits in the LSI range. This enables new types of electronic circuits, being lightweight, inexpensive, mechanically flexible, stretchable and energy efficient, that could be fabricated on demand through printing at small business places or even at home.

cfaed-1 success During cfaed-1, our scientists generated a number of world-leading results, especially in the area of single device design and electrical performance. Among these are a novel high current density vertical transistor with unrivalled current density (high kA/cm^2 regime) and transit frequency (>30MHz recently achieved) [2], and the first demonstration of an organic FET operating in inversion [3]. Furthermore, OFET devices and conducting polymer materials with record high mobility values and conductivities [4], and proof-of-concept devices with new materials such as 2D conjugated polymers were demonstrated [5-6]. Building on these significant advances at the material and device levels, OE will push towards demonstrator circuits containing up to hundreds of devices.

V-Targets OETag (cf. HITs): A unique, multifunctional, fully organic and printed demonstrator tag is explored combining sensor functionality, computing, wireless communication, positioning and power supply. We will design the organic optochemical sensors, which are used to enable the chemical analysis of materials. The sensed data can be processed by the printed processor unit comprising up to 10,000 transistors.

Why Dresden? Our team in Dresden has proven to be world class throughout recent years. We are the #1 location for organics in Europe and we have a proven track record in successful spin-offs.

B. *Reconfigurable Electronics Route "RE"*

Wall Today's electronics for computing rely on static devices and hardware. In arithmetic-logic-units (ALU) that build the basis for processors, for instance, information is routed to fixed functional blocks resulting in large inactive chip areas and considerable routing resources. In addition, a rigid separation between hardware (function) and software (command) results in a latency bottleneck as information is exchanged.

Approach Our approach of breaking those walls is to rethink the complete computation chain by enacting a flexible reconfiguration of hardware and enabling software defined hardware across all functional levels. We explore the unique window of opportunity that opens with reconfigurable Field Effect Transistors (RFETs). The functionality of the individual transistors is boosted from the current rigid and limited on/off switch function to enabling flexible reconfiguration between n- and p-type FETs, resulting in multiple deterministic functions as well as distinct logic operation and memory states.

The foundation of the RE Route is built on the successful work from cfaed-1 on Si nanowire RFET devices and circuits. The RFET merges two fundamental transistor types - electron- (n-channel) and hole- (p-channel) conduction - into one universal type of transistor allowing a flexible reconfiguration between either function [7] by a dedicated electric non-volatile program signal (cf. Fig. 5). Si and Ge nanowires are chosen as the vehicles to realize RFETs as they deliver the ultimate gating behavior [8] and show low integration barriers towards possible future implementation with the most aggressively scaled CMOS fabrication technology being currently developed for the sub-10 nm node at the industry level [9-10].

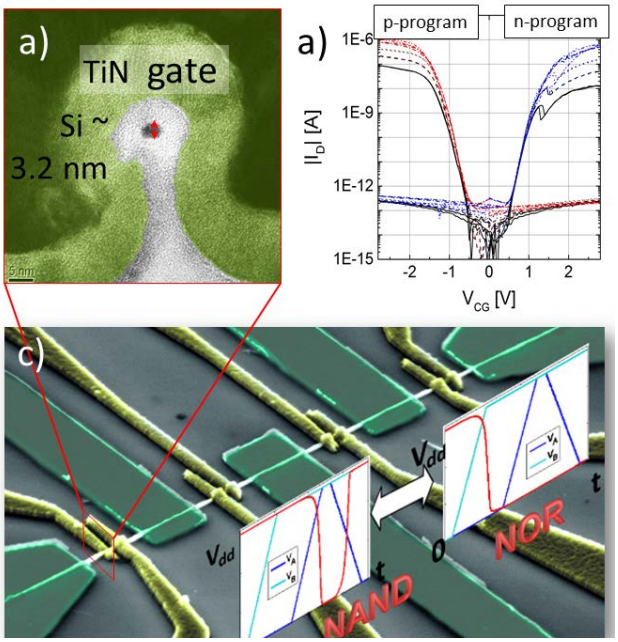

Fig. 5. Reconfigurable Si nanowire transistor. a) cross-section of device with omega gate and TiN electrode. b) Subthreshold transfer characteristics. c) 4T reconfigurable NAND-NOR cell with full output swing.

Benefit We expect benefits in substantial savings of power consumption, integration density and latency at the circuit and system levels as compared to CMOS benchmark systems. Inherent reconfigurability shall be exploited towards the design of hardware secure and resilient circuits as the functionality of these systems, i.e. the transistor's polarities, cannot be reversed engineered. With the fusion of memory and logic as well as non-volatile state memory enabled by ferroelectric HfO_2-based

gate stacks [11], zero-boot-time systems enter the realm of possibility. Digital sensing, i.e. sensors that are able to detect quantum events and output these events digitally, renders ADCs useless and therefore save chip area and power consumption.

cfaed-1 success The RFET results achieved in cfaed-1 have significantly shaped the field of reconfiguration of logic operation states by proposing and maturing the Si nanowire RFET. The RFET concept was first demonstrated with bottom-up Si nanowires [7]. Important experimental and theoretical advancements in nano-material science involving solid state reactions and strain engineering of nanowires [8] were implemented to yield a scalable and integratable device concept for the adjustment of drain-current symmetry between n- and p-program [12]. The drastic disparity of 10x otherwise found was lifted. This breakthrough has made cfaed symmetric RFETs the only devices of its kind to facilitate practical complementary circuits with runtime reconfigurability. The symmetric bottom-up technology was recently successfully transferred to a top-down SOI platform with omega shaped gate to enable Si nanowire based RFETs for device prototyping and circuit demonstration with a higher yield, and to proof compatibility of our technology with modern manufacturing [13]. Device performance limitations were initially identified [14] especially for specific realizations, e.g., the planar one in accordance to literature [15]. In response to that, performance boosting and reduction of dynamic power consumption strategies were found and demonstrated with bottom-up Ge nanowires and high-k / metal gate stacks and advanced gate architectures [16], [14]. To increase device functionality and to enable in-memory computing, we devised the multi-independent gate RFETs, adding more logic inputs without comprising on-conductance [17], [13] and included non-volatile and multi-bit operable reconfiguration features [18-19]. Inherent device reconfigurability was exploited at the circuit level, defining a library of fine grain reconfigurable logic cells, e.g. such as NAND/NOR/MIN or XOR/XNOR runtime reconfigurable functions [17], [14]. These efficient logic representations have seeded logic circuit opportunities as in multi-bit adders [20] and multiplexers [13]. A logic and physical synthesis flow from the application behavior level to the layout was set up [21] enabling the evaluation of the impact at the system level in terms of chip area, performance and critical delay paths.

V-Targets Our Route's V-Targets are to demonstrate disruptive innovations by bringing new fully hardware-reconfigurable ALUs, zero-boot-time systems as well as digital sensor circuits with ultimate resolution that cannot be executed with CMOS.

Why Dresden? Dresden is cradle and world leader in RFETs and HfO_2 based ferroelectrics. We have proven intra-disciplinarity starting from material science to disruptive device and circuit innovations and yielding into modern logic and physical synthesis flows. The local facilities together with the RE team make this activity in Dresden world-leading.

C. Spin-Orbit-Torque Electronics Route "SPOT"

Wall A major roadblock to advancing CMOS based computing systems are (1) scaling of existing memory technologies beyond the 10 to 20nm technology nodes (depending on the type of memory), (2) limitations on the size of these memories due to the innate physical structure of these memories, and (3) the need for a complex hierarchy of memory types that typically trade-off lower densities to achieve higher performance (speed and latency).

Approach Racetrack Memory (RTM) is a novel spintronic memory [22] that has a radically different operating principle than any charge-based memory – current or proposed – and which could allow for such a massive increase in high performance memory capacity whilst also offering non-volatility, and a reduction in the complexity of today's memory hierarchies. These unique properties can be realized by novel spin-orbitronic concepts, discovered only in the last three years. In particular, spin-orbitronics makes possible the motion of (antiferro-)magnetic domain walls in nanoscale structures at very high speeds exceeding 1km/s [23], thereby overcoming the limitations in propagation speed – and in magnetic domain size - that jeopardized the original RTM proposal [22][24]. Thus, Racetrack Memory now has very high potential as a unique memory concept.

The basic principle of RTM is that data is encoded in boundaries – the domain walls – between regions of opposite magnetization (red or blue regions in Fig. 5) in a magnetic nanowire that forms the racetrack. The presence or absence of the domain wall corresponds to a "1" or a "0". Most importantly, the domain walls are mobile and the data – a series of "0"s and "1"s – are moved synchronously, to and from, around the racetracks by spin-orbit torques generated via current pulses fed into the racetracks. Using vertical racetracks that have a cross-sectional area of just a few nm^2 and that are tall enough to accommodate 100 to 500 domain walls, RTM has the potential for memory capacities far exceeding any known solid-state memory today. In simple terms, RTM thus is the equivalent of a high capacity hard disk drive, but on a chip and with no moving parts. Moreover, RTM is innately 3D, with its major active components, the racetracks, being vertically oriented, unlike, for example, vertical FLASH which is a stacked 2D technology that limits improvements in density.

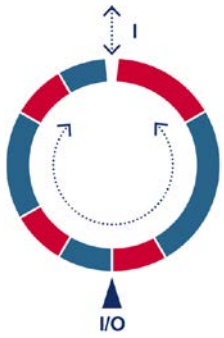

Fig. 5. Racetrack memory concept: A series of magnetic domain walls (boundaries between magnetic regions (red and blue) of opposite magnetization) are moved by current pulses (I) to an I/O device for reading and writing the domain walls.

Benefit Since RTM can uniquely trade off speed and latency, RTM has the potential to replace several of today's memories in one technology. This makes RTM attractive for future rPoF architectures (see HITs, section IV). Furthermore, RTM has the potential to increase the memory capacity close to the processor by 1 or 2 orders of magnitude and thereby significantly accelerate processing operation.

cfaed-1 success Over the past five years, major discoveries have led to a new major subfield of spintronics - spin-orbitronics - in which the phenomenon of spin-orbit coupling has led to novel and highly efficient means of creating pure spin currents.

V-Target Racetrack Memory: Exploiting our recent spin-orbit-torque breakthroughs and advancing beyond, we shall be able to monolithically integrate circular magnetic racetracks that will allow for domain wall bits that that can be driven in circles. Hence, one single read and write circuit shall be integrated to sequentially read/write a complete racetrack of, e.g., 128 bits. This shall allow for a breakthrough: monolithically embedding storage within circuits with a memory density of orders of magnitude beyond today's memories.

Why Dresden? Prof. Stuart Parkin, the inventor of RTM and 2014 Millenium Technology Prize winner, heads the team. We are leaders in spintronic materials and phenomena and in sprintronic circuit design.

D. Terahertz Electronics Route "THz"

Wall THz signal power generation at room temperature by either electronic or optical components presently suffers from poor device performance. Particularly, between 0.5–10THz the output power of both optics and electronics drops to very low levels. Similarly, signal detection in this THz gap (cf. Fig. 6) is plagued by high loss in the frequency conversion process.

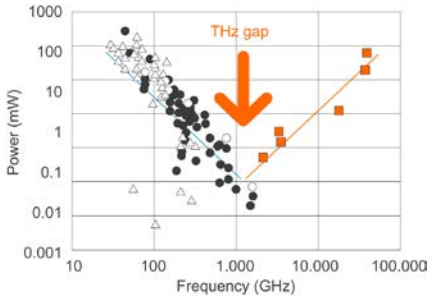

Fig. 6. The THz gap is generally defined by frequencies between 300GHz to 30THz (i.e. by wave lengths between 1mm and 10µm). (image: [25])

Approach Fig. 7 shows the cross section of an advanced npn HBT along with its relevant vertical layers and the carrier flow. According to the present roadmaps [26-27], the most critical issues limiting HBT performance are: increase of contact and series resistances with vertical and lateral scaling; vertical spreading of highly doped layers such as base and emitter; formation of parasitic energy barriers; leakage; thermal breakdown. Thus, this Route pursues two approaches in parallel: (i) circuit and system design using advanced HBT technology and (ii) exploring HBTs with new architectures and materials.

For both the transceiver and radar frontend, THz circuit and system concepts will be explored utilizing experimentally calibrated HBT models that enable circuit design at the process performance limit. For generating high power THz signals with high tuning range (i.e. bandwidth) we propose a novel quadrature oscillator topology where combining the phase shifted paths leads to frequency quadrupling. Reuse of inherent injection locking for frequency tuning will maximize oscillation frequency. Balancing peak oscillation frequency and tuning range with minimum phase noise will be aided by theory development. For THz transceiver-based communications systems, carrier recovery concepts will be investigated.

Sensitive detectors combined with high-power THz tuneable signal sources enable compact and extremely precise µm-scale resolution radar systems not being sensitive to dirt and dust. The requirements for realizing THz detectors are, among others, high responsivity, low noise, and lowest possible intrinsic and parasitic capacitances. Achieving these requirements favors 2D materials as well as 1D materials (preferably CNTs) from the aspect of their fundamental properties [28].

Possible 2D materials include, e.g., BP, GeS and other binary metal VI or IV-VI-compounds, which will be first screened for a high in-plane mean free path (at low field) by quantum chemical simulations. Promising candidate materials will be synthesized and experimentally characterized. Materials turning out to be suitable will then be integrated in actual detector structures with channel lengths below the carrier mean free path, which lets expect a strong interferometric enhancement of the sensitivity. Once a suitable channel material has been found, choosing proper contact materials and finding fabrication procedures for minimizing the contact resistivity will be addressed.

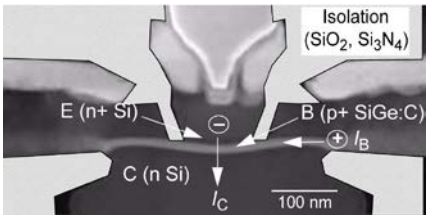

Fig. 7. TEM cross section of a 0.7THz SIGe:C npn HBT showing the relevant device regions and current flow directions.

Benefit Using ground-breaking approaches (e.g. specially tailored material layers) towards transistor, detector, and circuit design, our goal is to generate at least 1 mW of output power at 1 THz and room temperature. This shall enable a long list of new applications, including, among others, non-destructive material inspection (safety), extremely advanced medical diagnostics, radar for autonomous driving, and extremely high data rate wireless communications of 1 Tb/s and beyond.

cfaed-1 success HBT transistor modeling related research has led to the SiGe HBT roadmap (ITRS/IRDS) [26], while driving the highly successful EU projects DOTFIVE and DOTSEVEN (as Technical Project Manager) [29] has resulted in the most advanced SiGe:C HBT technology worldwide at IHP (Innovations for High Performance Microelectronics, Frankfurt/Oder/ Germany). The heterojunction bipolar transistor model HICUM has been an industry-wide standard since 2003 and is worldwide available in all commercial circuit simulators. High-frequency CNTFET expertise was documented in [30].

First-principles simulation capability (Gemming) has been utilized in cfaed for explaining experimentally observed conductivity changes in nanostructures [31][32] and can be applied to tailoring materials towards specific in- and out-of-plane transport properties. Antenna structures have been developed for Graphene based detectors working at frequencies ranging from 0.4THz up to 400THz [33] and structures for probing in- and out-of-plane transport properties have been fabricated [34].

V-Targets An oscillator with ≥1 mW output power: We will start our circuit design with this basic component for signal generation. Integrated radar front-end/wireless communications transceiver: Exploiting the new device and circuit design methodology jointly with our superior transistor modeling capabil-

ity, a THz emitter/detector "transceiver" and on-chip radar system for µm distance resolution shall be designed to operate at room temperature. For the first time, this shall enable commercially viable THz imaging, radar, as well as wireless communications.

Why Dresden? In our team in Dresden, we bring together long-term and complementary experience in devices, circuits, materials, fabrication, and systems.

E. Biomolecular Circuits Route "BIO"

Wall The rapid advances in electronics technology pose major walls with respect to the integration density of heterogeneous components, reliable operation despite unreliable components, and energy efficiency of both fabrication and operation. Biological systems - through billions of years of evolution - discovered unique solutions to these challenges on the level of molecules, cells and cellular networks. These solutions are fundamentally different from conventional electronic engineering approaches and often outmatch their performance in terms of size, energy efficiency, and resilience by orders of magnitude. The vision of this Route is to exploit these solutions for advancing electronics.

Approach Within the area of DNA-origami based optoelectronics, DNA-origami structures will direct the energy-efficient fab-free assembly of nano-objects into optoelectronic devices/circuits with massively reduced size and superior bandwidth. After assembly, DNA templates can be removed and devices/circuits can operate in a dry environment for on-chip computations. The produced optoelectronic devices/circuits are 100-1,000 times smaller than currently used elements (e.g. waveguides, modulators, antennas).

We will also tackle dynamic self-organization of biomolecules in wet environments exploiting two complementary strategies:

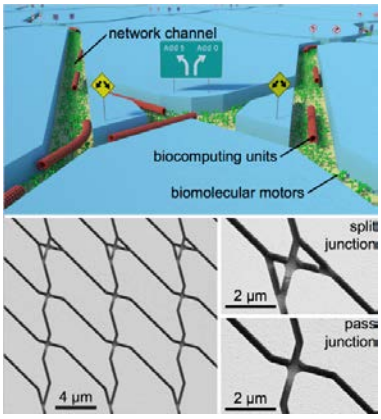

Fig. 8. Schematic of a programmable molecular-motor based computer

Our approach "Programmable molecular-motor based computer" (cf. Fig. 8) harnesses biomolecular transport to solve specific computational problems with substantially increased energy efficiency. Another approach, "Robust biomolecular signal processing" (cf. Fig. 9), exploits signal processing by collectively interacting biomolecules and bridging it with wet multimodal sensing to yield a robust biomolecular near-sensor processor that directly senses multichannel input in wet environments at few-molecule resolution. Of course, these systems shouldn't be standalone but integrated with conventional CMOS technologies providing guidelines for their rational design and translating generic bio-concepts to other routes. As functional DNA-origami structures can be operative in biomolecular signal processing systems and in optoelectronic functional elements, they will serve as an interface between 'wet-state' and 'dry-state' electronics. Thus, the molecular sensitivity and collective processing capabilities of biochemical signaling will enable true bio-hybrid processing

Benefit If we succeed with our approach of DNA-origami based optoelectronics, we expect 100x denser high-bandwidth optoelectronics. Furthermore, our Route shall result in enabling

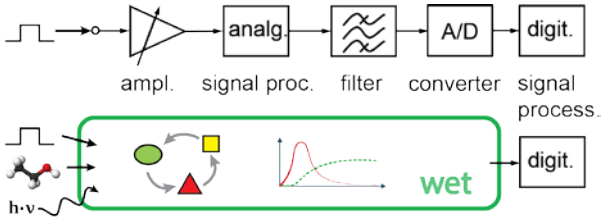

Fig. 9. The biomolecular near-sensor processor operates next to biomolecular sensors and simultaneously replaces sequential processing by standard engineered routines such as amplifier, analog signal processing, filter and A/D converter. It directly provides robust decision signals in response to multichannel inputs, even at few-molecule resolution

robust bio-molecular sensors and processors for new applications, e.g., in food and health, and, in particular for complex multi-channel sensing and low-energy processing under harsh energy constraints.

cfaed-1 success We were first to use DNA origami for templating nanoparticles into plasmonic waveguides [35-36] and motor proteins for low-energy computing [37]. We discovered fundamentals of molecular decision making of cells [38], now to be used for electronics.

V-Targets Plasmonic waveguides: Innovating on DNA templating, we shall enable 100x density improvements on optical chip-to-chip interconnects. Bio-hybrid computing: Innovating on our synthetic motor protein circuits, we plan to show 100x energy improvement for difficult computational tasks. Multichannel biomolecular sensing: Incorporating our understanding of decision-making in a bio-sensor, we will build first bio-molecular hybrid sensing and signal processing circuits.

Why Dresden? Our team spans all layers from materials to systems level and includes scientists from all necessary research fields: biology, physics, materials, and engineering.

F. Orchestration Route "ORCH"

Our previous five Routes reach across layers from materials to circuits, exploiting fundamentally new concepts. Above the circuits layer, in ORCH, we envision a radically new system architecture with hardware reconfiguration everywhere, blurred boundaries between computing and memory, an extreme dense storage, acceleration via unconventional computing approaches, and unprecedented communication throughput. To make such a complex system usable, we jointly co-design novel hardware and software architectures. To this end, we follow a model-based approach that enables a systematic design space exploration. This is fascinating new ground, open for exploration with a perspective of adaptivity and efficiency, far beyond those of today's computing systems.

Wall Two walls need to be tackled. (1) Ever-widening HW-SW gap: The rapid increase in software (SW) complexity with numerous layers of abstraction and the pace of innovation in HW architectures make it difficult to exploit the full potential of computing systems. This is aggravated by the high disruption potential of novel cfaed technologies. Without jointly architecting HW and SW, the gap may become unsurmountable, rendering technological innovation of no use for applications. (2) Systems design wall: Classical architectures, including von-Neumann approaches, comprise separate computing, memory, interconnect and sensing components. This "systems design wall" hinders cfaed's materials-inspired innovations, which enable breaking classical component boundaries, to come to full fruition.

Approach In ORCH, we propose a hardware and software system-level research to unleash the full potential of new technologies developed by the materials-inspired Routes, in particular: (OE) We conceive a design framework aware of fabrication constraints such that organic electronics can be targeted efficiently. (RE) We exploit reconfigurable electronics via a new kind of reconfigurable fabric that allows switching among instruction set architectures to adapt to the workload at runtime. (SPOT) We develop ways to embed reconfigurable racetrack memories within as well as around the reconfigurable logic fabric. (THz) We contribute to integrating beyond 10 Tb/s I/O bandwidth enabled by THz transceivers. (BIO) We show a path to systems concepts exploiting dense optical interconnects and low-energy motor-driven filament accelerators with a new dimension of heterogeneity for unchallenged new applications.

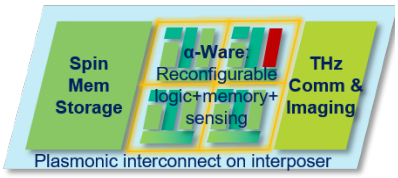

Fig. 10. α-Ware sketch

Our scientific approach is based on a system-level model-based HW/SW co-design methodology that imports early device models from the materials-inspired Routes and exports system-level insight to help steer development in physics, chemistry, material sciences and circuits. The main characteristics will be extracted from lower-level models of future components and translated into higher level operational models with quantitative annotations. The symbiotic effects of combining new technologies into a system will be investigated and optimized by dependability analysis, simulation and probabilistic model checking. This will allow us to perform HW/SW co-design and systematically rethink HW and SW architectures.

We envision a novel fabric with unprecedented reconfigurability and dissolved boundaries between memory, logic and sensing for unchallenged new applications, which we call **α-Ware** (cf. Fig. 10). With α-Ware, we leverage the technologies of the materials-inspired Routes: (1) new device reconfigurability (RE), (2) memory-in-logic (RE), (3) extremely fast local RTMs and dense storage-class RTMs (SPOT) as well as new register files, (4) wet computing for analog near-sensor computing and acceleration of computationally hard problems (BIO), and (5) extremely fast and energy efficient interconnect (BIO) in collaboration with HAEC. α-Ware will break the systems design wall and open up new possibilities for HW/SW architectures. For example, fast logic reconfiguration will allow changing the data path close to memory, instead of moving data to the right data path, whereas RTM may flatten the memory hierarchy, making architectural innovations obsolete that hide memory latencies (e.g., certain types of caches or HW multi-threading). This, in turn, will lead to a new system SW, e.g., (1) simplified memory management by the Operating System (OS), (2) novel resource management for reserving areas of the α-Ware while ensuring isolation, and (3) novel languages and compilers that not only program but also define the architecture. These kinds of system SW considerations will use a systematic knowledge-based representation of system resources at design-, compile- and run-time. Only by jointly developing HW/SW architectures around cfaed technologies will we unleash the device breakthroughs at system level, disrupting the otherwise incremental innovation paradigm.

Benefit The expected benefits consist of measurable improvements for end-user applications, unleashing their full potential to the application cause. cfaed will not only deliver exciting devices and circuits but will also demonstrate their impact on real applications. Beyond the benefits of single technologies, we expect systems research in ORCH to lead to synergistic effects, e.g., combining embedded RTMs close to reconfigurable logic. Novel resource management at different levels such as intelligent data placement to RTMs will make SW considerably more efficient. Compared to classical SW systems for certain application domains (e.g., big data or wireless communications), we expect orders of magnitude improvement in selected figures of merit such as energy efficiency, area or performance.

cfaed-1 success We developed the concept of a wildly heterogeneous system design, incorporating software design concepts, operating systems, kernel scheduling for heterogeneous multi-processor systems as well as a resilient network-on-chip [39]. All was proven by designing and testing multiple "Tomahawk" chips fabricated in current CMOS [40].

V-Targets α-Ware: We will build multiple instantiations of our radically new processing platform ("α-Ware") and benchmark it using system-level simulation techniques. At the system level, this will allow us to quickly observe the impact of new software architectures, and of changes at the device and circuit level from Routes A-E (captured by their V-Targets). Early system-level analysis within cfaed will enable large leaps in technology viability and adoption, disrupting the otherwise incremental innovation paradigm.

Why Dresden? We bring together a strong interdisciplinary team with a proven track record, very strong in HW/SW design, theory and applications.

IV. Horizontal Integration Targets "HITs"

To foster interplay and coherence between the Routes, as well as to show additional potential when combining the results, we introduce "Horizontal Integration Targets" (HITs, cf. Fig. 2). The HITs are crucial for multiple Routes that join forces to achieve common systems goals.

G. Reconfigurable Processor-of-the-Future (rPoF)

Today, many different kinds of processors exist, e.g., DSPs, GPPs, MPUs, GPUs, just to name a few. Also, processor design frameworks exist that allow to add acceleration and custom instructions to make processors more efficient for a specific application area. We envision a whole new processor platform to be developed by exploiting the reconfigurability enabled by the RE Route, embedding Racetrack Memories of the SPOT Route, and Tb/s wideband I/O as enabled by the THz Route. By designing a "reconfigurable Arithmetic Logic Unit", for example, an rPoF can reconfigure every single clock tick from one instruction set to another, enabling unheard flexibility, and thereby fueling ORCH's research goals. Finally, the rPoF shall also be implementable in a non-reconfigurable way that incorporates the constraints of organic electronics from the OE Route (cf. OETag below).

H. Organic Electronics Tag (OETag)

Exploiting the rPoF HIT framework, we can generate specific hardwired processor versions targeted for organic electronics. By the exchange of results from OE/RE/ORCH Routes, we want to demonstrate printed individualized processors. Improving on the transit frequency achieved within cfaed-1, we shall be able to add the world's first printable active radio frequency interface. Adding sensing, an individualized tag "OETag" shall become feasible, allowing it to sense and tag objects as needed, and printed on-demand.

I. Highly Adaptive Energy Efficient Computing (HAEC)

Within cfaed-1, we did not have dedicated HITs but used CRC HAEC (separately funded DFG collaborative research center) to benchmark our results. Within cfaed-2, we will continue cooperation with HAEC, in particular to show the benefits of the BIO and THz Routes' outputs. With the explosion in the number of compute nodes, the bottleneck of future computing lies in the network architecture connecting the nodes. Addressing the bottleneck lies in replacing current rack backplanes. HAEC proposes to revolutionize computing electronics by realizing embedded optical waveguides for on-board networking, and wireless chip-to-chip links at 200 GHz carrier frequency connecting neighboring boards in a rack. This shall drive current backplane rates from Tb/s to Pb/s orders of magnitude. Driven by new interconnects using our plasmonic interconnects of the BIO and THz Route's output, we envision backplanes in the range of Eb/s. This extends the futuristic vision of HAEC by orders of magnitude. Incorporating ORCH's processing platform would enable innovation in edge cloud computing for future cellular communications for decades to come.

V. SUMMARY

In this paper, we outlined the approach of cfaed (Center for Advancing Electronics Dresden) for advancing electronics beyond the IRDS roadmap into unclaimed territory. We identified six Research Routes, in which we believe we can demonstrate outstanding potential through our excellence in Research and our favorable setting in Dresden. Our research measures brought in place for achieving our objectives are (1) vertical "bridging" of layers across materials, devices, circuits and systems through V-Targets as well as (2) horizontal coherence in research across our six Research Routes through Horizontal Integration Targets that combine the individual research outcomes to a system never seen before. Together, in a truly unique interdisciplinary manner, we will venture electronics into unknown grounds.

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