Signal-to-Noise Ratio of Direct Sampling Receivers with Realistic Sampling Circuit Models

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Abstract—Employing direct sampling receivers for multi-mode multi-band operation in mobile communications is advantageous due to their high flexibility and programmability. But this type of receiver needs to be properly adjusted regarding the parameters of the sampling and the quantization stage of the analog-to-digital converter to comply with certain performance requirements.

This paper studies the impact of the ideal, the track-and-hold and the sample-and-hold sampling circuit on the effective in-band signal-to-noise ratio of the receive signal. It also proposes sets of valid parameters of the complete analog-to-digital converter in terms of the duty cycle, the sampling rate, and the quantization resolution for a given band-pass input signal to limit the maximum performance loss. Moreover, the investigations for the different samplers and the overall analog-to-digital converter are used to trade-off the individual parameters in case of an exemplary LTE signal reception.

I. INTRODUCTION

The technological evolution in wireless communications continues and mobile receiver terminals have to support a variety of communication standards. Enabling multi-mode multi-band (MMMB) receivers for cognitive radios is an enormous challenge. Here, the ability to select a variety of frequency ranges to ensure flexibility, while keeping the involved power consumption of the analog and digital frontend low, is the key. A comprehensive study of available techniques for MMMB transceiver design and realization issues is given in [1].

One promising approach, following Mitola’s vision [2], is direct sampling of band-pass signals. It reduces the complexity of the analog receiver frontend (AFE) and shifts some of the signal processing tasks, e.g., down-conversion and low-pass filtering, to the digital domain with the benefit of reduced size, cost, and power consumption of the receiver.

To adopt the direct sampling approach in a feasible receiver architecture, its performance in terms of signal-to-noise ratio (SNR) has to be studied. Especially, the impact of realistic sampling circuits, which are part of the analog-to-digital converter (ADC) stage and may influence the performance significantly, has to be considered carefully. In [3], two realistic sampling circuit models, the voltage and charge sampler, are compared with respect to their transfer function, clock jitter, and noise characteristics. An extension of the charge sampler by an embedded filter function is proposed as an attractive approach for direct RF sampling. This has been extended to a programmable band-pass charge sampling mixer, which combines the functionality of a homodyne mixer and baseband sampler, in [4]. The basics of charge sampling, mainly used in integrated circuits, are discussed in [5]. An accurate model of a sample-and-hold circuit with limited integration/aperture time together with the analysis of its transfer function and phase response is given in [6].

In this paper, previous analysis (cf. [7]) is extended by investigating the behavior of the SNR performance of the realistic sampling circuits and the overall ADC with a strong focus on sub-sampling applications. The system model of the direct sampling receiver (DSR) is shown in Fig. 1. The proposed sub-sampling ADC consists of two separate parts. First, the sampling circuit modeled as a combination of a linear filter \( h_s(t) \) and an ideal sampler. Second, the quantization unit \( Q(\cdot) \) with a variable resolution \( b \). Moreover, guidelines to determine suitable parameterization of the ADC are presented. Adjustable parameters are the duty cycle \( d \), the sampling rate \( f_s = 1/T_s \), and the quantization resolution \( b \).

The remainder of this paper is organized as follows: Section II introduces three sampling circuits and specifies the derived linear system model. Section III covers the impact of the sampling circuits on the SNR performance of a band-limited input signal. The analysis is extended for the complete ADC including the quantization distortion for an exemplary LTE scenario in Section IV. Conclusions are drawn in Section V.

II. SYSTEM MODEL

Direct sampling of continuous-time band-pass signals is based on the aliased spectrum of the signal in order to translate the input signal to an intermediate frequency and sample it in the first Nyquist zone. The sampling rate \( f_s \) of the DSR is generally lower bounded by \( 2B \leq f_s \) to fulfill the Nyquist

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criterion as derived in [8]. Here, the bandwidth of the desired signal is denoted as \( B \).

Furthermore, technological constraints may limit the maximum sampling rate and lead to rates smaller than the Nyquist frequency \( f_s < f_{\text{nyq}} = 2 \cdot f_c + B \). This sampling technique is commonly known as sub-sampling. It has been studied for band-limited band-pass signals in [9]. Apart from this, an appropriate sub-sampling rate \( f_s \) has to comply with a second condition to ensure an aliasing-free signal spectrum:

\[
\frac{2f_c + B}{n} \leq f_s \leq \frac{2f_c - B}{n - 1},
\]

where \( n \) is defined as \( n \in \mathbb{N}^+ \leq \left[ \frac{2f_c}{B} \right] + 1 \).

Now, a normalized sub-sampling factor shall be defined as \( F_{\text{sub}} = \frac{f_{\text{ref}}}{f_s} \) given that a reference sampling rate is given by \( f_{\text{ref}} \geq f_{\text{nyq}} \). This factor is used to compare the SNR performance of a conventional Nyquist receiver with \( f_s \geq f_{\text{nyq}} \) to the sub-sampling receiver \( f_s < f_{\text{nyq}} \).

Both architectures have to apply a proper band selection filter in advance, e.g., to remove coexistent radio systems or adjacent bands, and to sustain an adequate system performance. For MMBB radios, filters require to be highly flexible with the opportunity to adjust individual parameters.

A strong impact on the SNR performance of the sub-sampling receiver emerges from the used sampling circuit. This shall be discussed in the following.

A. Ideal Uniform Sampling

Assume an ideal uniform sampling process with a period \( T_s \). Ideal sampling is modeled as the multiplication of the time-continuous input signal \( r(t) \) with an impulse train function \( \Delta_{T_s}(t) = T_s \cdot \sum_{k=-\infty}^{\infty} \delta(t - kT_s) \), such that the sampled signal is expressed as \( x(t) = r(t) \cdot \Delta_{T_s}(t) \). This ideal model does not distort nor attenuate the input signal during it is shifted from any higher Nyquist zone to the first Nyquist zone.

Given that the input signal \( r(t) \) contains an additive band-limited white Gaussian noise component \( n(t) \) with a cut-off frequency \( f_N > f_s \) higher than the sampling rate.

It can increase the noise power density in the frequency range of interest due to the effect of noise folding [9]. The resulting signal-to-noise ratio (SNR) in the desired band is affected such that the effective in-band SNR \( \gamma_s \) at the output of the ideal sampler is decreased. It decreases by about 3 dB as compared to the in-band SNR \( \gamma_{\text{in}} \) at the sampler input when halving the sampling rate \( f_s \) (cf. [9]). The general relation between input and output is formulated as:

\[
\gamma_s = \frac{\gamma_{\text{in}}}{F_{\text{sub}}},
\]

It assumes that the cut-off frequency of the band-limited noise is \( f_N = f_{\text{ref}}/2 \) and \( F_{\text{sub}} \in \mathbb{N}^+ \).

The presented ideal uniform model is often used to introduce the sampling theory in literature. But it neglects the frequency-dependent characteristics of realistic sampling circuits. Especially for sub-sampling applications, these characteristics are important and have to be taken into account to limit the performance degradation.

B. Uniform Sampling with Realistic Sampling Circuits

Two realistic sampling circuit models are commonly used: the track-and-hold (TH) and the sample-and-hold (SH) sampler. A comprehensive survey of various types of sampling circuit implementations is available in [10].

For the TH, the input signal (voltage) faces a first order RC circuit when the switch \( S_1 \) is closed. The switch closes periodically with the sampling period \( T_s \) and opens after a predefined time interval \( T_1 \). During the hold phase \( (S_1 \text{ is open}) \), the voltage over the sampling capacitor \( C_{\text{H}} \) is read by subsequent processing units, e.g., the quantization circuit. The TH circuit does not need to discharge the capacitor between consecutive periods, but therefor the RC time constant \( \tau \) has to be chosen adequate \( \tau \ll T_1 \) to ensure mutually independent samples. The TH circuit, which is often referred as a voltage sampler (cf. [3]), is operating almost like an ideal sampling circuit given that the RC time constant satisfies \( \tau \ll T_1 \).

For the SH circuit, the input signal (voltage) is converted into an equivalent current by an transconductance amplifier with fixed conductance first. The capacitor \( C_{\text{H}} \) is charged as long as \( S_1 \) is closed. During the hold phase, the switches \( S_1 \) and \( S_2 \) are open and the voltage of the capacitor is read. At the end of each sampling period, \( S_2 \) is closed to discharge the sampling capacitor \( C_{\text{H}} \).

For both architectures, the ratio of the sampling time \( T_1 \) to the overall sampling period \( T_s \) defines the duty cycle \( d \):

\[
d = \frac{T_1}{T_s} \in (0, 1].
\]

A common value of the duty cycle is \( d = 0.5 \). Increasing the sampling rate \( f_s \), and hence decreasing the time period \( T_s \) makes it more and more complicated to ensure proper scaling of the time constant \( \tau \). This strongly influences the characteristics of the sampled signal.

A system model shall be formulated to analyze this impact on the effective in-band SNR of realistic sampling architectures. It extends the ideal model from Sec. II-A by an antecedent linear filter \( h_s(t) \) as shown in Fig. 2.

![Fig. 2: System model of the realistic sampling circuit.](image)

Here, the impulse response \( h_s(t) \) of the filter accounts for the characteristics of the realistic sampling circuit (most likely low-pass). The output signal is formulated as

\[
x(t) = [r(t) * h_s(t)] \cdot \Delta_{T_1} (t - T_1)
\]

in time domain and

\[
X(f) = |R(f) \cdot H_s(f)| \cdot \left[ \Delta_{\frac{T_1}{2}} (f) \cdot e^{-j2\pi f T_1} \right]
\]

in frequency domain, respectively. It shows that the desired input signal \( r(t) \) is first distorted by the filter \( h_s(t) \) of the circuit and than sampled at time instances \( t_k = k \cdot T_s + T_1 \).
Referring to the low-pass characteristics of the considered sampling circuits, the 3 dB bandwidth is a commonly used parameter. It follows from the RC time constant $\tau$ as:

$$\frac{f_{\text{3dB}}}{f_s} = \frac{1}{2\pi\tau} \cdot \frac{1}{f_s} = \frac{1}{2\pi\tau} \cdot \frac{T_1}{d} = \frac{\nu}{2\pi d}. \quad (6)$$

Here, the time constant $\tau$ and the integration time interval $T_1$ are interrelated by $T_1 = \nu \cdot \tau$, where typically $\nu \gg 1$.

For the TH circuit, the time domain behavior ($S_1$ closed) is similar to a first order RC low-pass filter with a limited integration time interval $T_1$ (cf. [6]):

$$h_a(t) = \frac{1}{\tau} e^{-t/\tau} \quad t \in [0, T_1]. \quad (7)$$

According to [6] and applying (6), the transfer function $H_s(f) = |H_s(f)| \cdot e^{j\phi(f)}$ of the sampling circuit derives as:

$$|H_s(f)| = \sqrt{\frac{1 + e^{-4\pi d f_{\text{3dB}}/\nu} - 2e^{-2\pi d f_{\text{3dB}}/\nu} \cos(2\pi d f_T)}{1 + \left(\frac{f}{f_{\text{3dB}}}\right)^2}}.$$  

$$\phi(f) = \arctan \left(\frac{e^{-2\pi d f_{\text{3dB}}/\nu} \sin(2\pi d f_T)}{1 - e^{-2\pi d f_{\text{3dB}}/\nu} \cos(2\pi d f_T)}\right). \quad (8)$$

Now, (8) is simplified under certain assumptions on the carrier frequency $f_c$, the bandwidth $B$ of the input signal, and the type of the sampling circuit.

For the TH circuit and input signals, only containing frequencies much lower than the 3 dB bandwidth of the sampling circuit $f_c < f_{\text{3dB}}$ ($\tau \to 0$), the effective transfer function can be approximated as $H_s(f) = 1$. This approximation corresponds to the ideal sampler from Sec. II-A.

For narrow-band input signals which are situated closely to or even higher than the 3 dB bandwidth ($f_c \approx f_{\text{3dB}}$) and which are sampled at a rate of $f_s \approx 2 \pi f_{\text{3dB}}$ ($\tau < T_1$), the sampling circuit shows a typical RC low-pass characteristic:

$$|H_{s,\text{TH}}(f)| = \frac{1}{1 + \left|\frac{f}{f_{\text{TH}}}\right|^2}. \quad (9)$$

$$\phi_{\text{TH}}(f) = -\arctan \left(\frac{f}{f_{\text{3dB}}}\right) \quad (10)$$

For the SH architecture, the transfer function has a sinc-shaped spectrum due to the integration of the charge in the sampling capacitor $C_H$ over the time interval $T_1$. The integration of the input signal coincides to the convolution of the input signal $r(t)$ with a filter function $h_a(t) = 1$ for $t \in [0, T_1]$ as derived in (4) given that $f_s \gg 2\pi d f_{\text{3dB}}$ ($\tau \gg T_1$):

$$|H_{s,\text{SH}}(f)| = \frac{2\pi d \cdot f_{\text{3dB}}}{f_s} \cdot \text{sinc} \left(\frac{f_{\text{3dB}}}{f_s}\right). \quad (11)$$

$$\phi_{\text{SH}}(f) = \arctan \left(\frac{\pi d f_{\text{3dB}}}{f_s}\right) - \arctan \left(\frac{f}{f_{\text{3dB}}}\right).$$

Here, $\sin(x) = \frac{\sin(\pi x)}{\pi x}$. Note that we do not consider the case of a RC time constant $\tau \approx T_1$ for the TH circuit because this would be contradictory to the assumption of mutually independent samples.

The obtained results are used to study the SNR performance of a sub-sampling circuit in the next section.

### III. Performance Evaluation of Both Sampling Circuits

The linear system model is the basis for the performance evaluations of the ideal, TH, and the SH circuit. It allows to be parameterized in the sampling frequency $f_s$, the duty cycle $d$, and the 3 dB bandwidth $f_{\text{3dB}}$ (inherently dependent on $\tau$) for various input signals. The applied performance metric is the resulting effective SNR $\gamma_s$ in the frequency band of interest. The output signal is $x(t) = x_s(t) + x_n(t)$, i.e., it consists of the useful signal and an additive noise term. The effective SNR is defined as the ratio of the useful signal power $P_{x_s}$ to the in-band noise power $P_{x_n}$:

$$\gamma_s(f, B, f_s) = \frac{P_{x_s}}{P_{x_n}} = \frac{\int_{f_{\text{1}} + B/2}^{f_{\text{1}} + B/2} S_{xx}(f) \, df}{\int_{f_{\text{1}} + B/2}^{f_{\text{1}} + B/2} S_{nn}(f - f_0) \, df}, \quad (11)$$

where $S_{xx}(f)$ is the power spectral density (PSD) of $x(t)$. Furthermore, no self-aliasing of the desired signal is assumed due to the correct choice of $f_c$ as discussed in Sec. II.

The input signal is considered to be a band-limited Gaussian signal $s(t)$ with a given carrier frequency $f_c$ and bandwidth $B$ plus an additive white Gaussian noise source $n(t)$. The Gaussian statistics are reasonable for OFDM transmission with a certain amount of sub-carriers. The lowest and highest frequency of $s(t)$ is defined as:

$$f_1 = f_c - B/2, \quad f_u = f_c + B./2. \quad (12)$$

The desired signal and the noise are filtered by a low-pass filter with impulse response $h_{\text{AFE}}(t)$ (see Fig. 1). The filter has a constant attenuation in the passband, a cut-off frequency of $f_{\text{cut}} \geq f_c + B/2$ and models the characteristic of the analog receiver frontend ($AFE$). Finally, the input signal $r(t) = r_r(t) + r_n(t)$ at the input of the sampling circuit shall be specified by its in-band SNR $\gamma_{in}$.

Considering the sampling circuit model as shown in Fig. 2 allows us to formulate the effective SNR $\gamma_s(f, B, f_s)$ at the output of the sampler as a function of the input signal. At first, a constant power spectral density of the desired signal $S_{rr}(f)$ and the noise component $S_{nn}(f)$, respectively, allows to simplify the integration from (11). Moreover, the band-limitation of the noise due to $h_{\text{AFE}}(t)$ limits the overall noise power in the system. Hence, the spectral density of the noise raises to at most $F_{\text{sub}} = \frac{\pi}{2f_s}$ times the noise density of $r_n(t)$. 

This leads to the final expression of the effective in-band SNR of the sampling circuit:

\[ \alpha_s (\gamma_{in}, d, f_s) = \gamma_{in} \cdot \frac{\int_{f_s}^{f_s+8} |H_s(f)|^2 df}{\int_{f_s}^{f_s+8} |H_{SH}(f - i f_s)|^2 df}. \]  

(13)

The SNR degradation \( \alpha_s \) is independent from the input SNR \( \gamma_{in} \). It shall be used to study the performance of the different sampling circuits numerically.

The degradation \( \alpha_s \) is shown for two exemplary sampling rates in Fig. 3 and Fig. 4. The parameters of the considered system setup are specified in Tab. I.

It can be seen in Fig. 3 that all samplers perform best for \( d \rightarrow 0 \) (ideal case). For all other cases of \( d \), the ideal sampler has the lowest degradations, while the SH has the highest loss in the SNR. The TH is situated in-between, depending on its 3 dB bandwidth (defined by the ratio \( T_f / \tau \)). The SNR shows a high degradation for two particular duty cycles (\( d \approx 0.5 \) and \( d \approx 1 \)). In these cases, the transfer function \( H_{s,SH}(f) \) has zero crossings at the carrier frequency \( f_c \) of the input signal. This setup should be avoided in an receiver design.

Fig. 4 shows that lower the sampling rates, which corresponds to higher sub-sampling factors \( F_{sub} \), increases the losses. Furthermore, it can be seen that the duty cycle \( d \) has to be carefully chosen to minimize the loss in signal quality.

Summarizing the obtained results, we conclude that the SH circuit shows highest degradations in the SNR as compared to the TH circuit and also to the ideal sampler. Given that the 3 dB bandwidth can be designed properly, the TH circuit is therefore most advantageous for sub-sampling applications.

**IV. Application Example**

The application example incorporates the derived linear sampling model from Fig. 2 into a general representation of the overall sub-sampling ADC. It includes the limited quantization resolution \( b \). In this section, the effective SNR of the ADC shall be evaluated and feasible parameterizations shall be obtained. Results for the system model, as shown in Fig. 1, are discussed.

The quantization operation \( Q(\cdot) \) is modeled according to the pseudo quantization noise model (cf. [11]). An additional scaling factor \( \zeta \) (cf. [7]) adjusts the signal-to-quantization noise ratio (SQNR) for low-quantization resolutions. It allows us to derive the SQNR \( \gamma_q \) of the quantizer as a function of its resolution \( b \), the oversampling ratio \( f_s / B \), and the peak-to-average-power ratio \( \eta_x \) of \( x[n] \):

\[ \gamma_q \left( b, \frac{f_s}{B}, \eta_x, \zeta \right) = \frac{1}{\zeta} \cdot 3 \cdot 4^b \cdot \frac{f_s}{B}. \]

(14)

Using the results from Sec. III and from (14) allows to formulate the effective in-band SNR of the DSR as

\[ \gamma_{eff} (\gamma_{in}, d, f_s, b) = \frac{\alpha_s (\gamma_{in}, d, f_s)}{\gamma_s (\gamma_{in}, d, f_s)} \gamma_q (b) + \alpha_q (b) + 1. \]

(15)

The following assumptions have to be made prior to the evaluations. The equivalent noise bandwidth of the AFE is defined by \( h_{AFE}(t) \) and does not change with \( f_s \). Furthermore, the decision levels and output values of the quantizer are determined by minimizing the mean square quantization error [12].

Based on (15), valid parameter sets can be found to achieve a certain system performance. To obtain a valid parameters for the duty cycle \( d \), the sampling rate \( f_s \), and the quantization resolution \( b \), a suitable performance metric is formulated. The used metric is defined as the maximum allowed in-band SNR loss \( \alpha \) in linear scale due the sub-sampling ADC:

\[ \alpha = \frac{\gamma_{eff}}{\gamma_{in}} < 1. \]

(16)
Fig. 5: Worst case parameterization of the sub-sampling factor $F_{\text{sub}}$ and the quantization resolution $b$ of the DSR employing a TH sampling circuit with $T_i = 3\tau$, a given SNR loss of $\alpha = 5, 10$ dB, a duty cycle $d = 35, 50\%$, and an in-band SNR $\gamma_{ib} = 50$ dB of the input signal.

![Figure 5](image)

It allows to find feasible configurations of the parameters $(d, f_s, b)$ for given values of $\alpha$.

Again, consider the system parameters from Table I for a sub-sampling ADC. The relation between sub-sampling factor $F_{\text{sub}}$ and quantization resolution $b$, given that the SNR loss is set to $\alpha = 5, 10$ dB, is shown in Fig. 5. The solid and the dashed lines are representing the worst-case configuration of the sub-sampling ADC. For both cases, we can observe that the sub-sampling factor $F_{\text{sub}}$ has to be chosen lower for $d = 35\%$ as for $d = 50\%$. The main reason is the higher noise contribution as discussed in Sec. III. earlier.

In Fig. 6, the effective in-band SNR $\gamma_{\text{eff}}$ of the sub-sampling ADC is shown as a function of the duty cycle $d$ given that the quantization resolution is fixed to $b = 8$ bit. Again, the SNR loss is defined as $\alpha = 10$ dB and the input SNR is $\gamma_{ib} = 50$ dB. It can be observed that duty cycle $d$ of both sampling architectures has to smaller than 50% to met the SNR constraint. Furthermore, the SNR degrades much faster for the SH compared to the TH and a sub-sampling factor of $F_{\text{sub}} > 4$ is not feasible in practice.

This analysis has shown that there are a multitude of feasible solution sets $(d, f_s, b)$ to configure the DSR for a given input signal and a maximum SNR loss $\alpha$. The present results providing a worst-case parameterization of the sub-sampling ADC. Further restrictions, as for example certain constraints on the power consumption, have to be integrated in the future to limit the amount of possible solutions.

V. CONCLUSIONS

This paper has modeled and analyzed the impact of one ideal and two realistic sampling circuits on the effective in-band SNR performance of a sub-sampling ADC. In the first part, the linear model for the ideal, TH, and SH sampling circuit is presented and analyzed with a focus on sub-sampling applications. It has been shown, that the correct choice of the duty cycle improves the performance of the receiver significantly. For example, the SNR loss can be reduced by about 23 dB if the duty cycle is changed from $d = 0.5$ to $d = 0.38$ as shown in Fig. 4. The SNR $\gamma_{ib}$ has been used to expand the analysis for the complete sub-sampling ADC including quantization to determine a valid parameterization of the ADC. It extends the results previously published in [7]. Here, it has been discussed for an exemplary LTE system where the duty cycle, the sampling rate, and the quantization resolution have been traded-off carefully. The methodology and the obtained results can be used to determine valid parameterizations of a sub-sampling ADC for various input signals.

REFERENCES