HW/SW Co-Design Lab

Seminar 1

WS 2017/2018
Schedule of the Lab

Introduction:
Become acquainted with software and tool flows

Lab task:

Internet: http://mns.ifn.et.tu-dresden.de/Teaching/Courses/Pages/P-HWSW-Codesign.aspx

Work:
Autonomous work in groups of 2-3 people
during WS in our PC pools and preferably on your own PC due to limited seats in PC pool

Delivery:
During WS: until 31st March 2018
1. Exported project workspaces including all sources (C, TIE)
2. Project report: Word-Template on Website

Hand in via e-mail: sebastian.haas@tu-dresden.de

Evaluation: Grade for 0/0/2 course, ET/IST: Lecture+Lab 7 credits, NES: 4 credits

Do not forget to register for the lab via HISQIS before examination period starts!
Tasks

1. FIR filter
   - Develop instruction set extensions for Tensilica processor (TIE)
   - Use Fusion, SIMD, FLIX
   - Compare direct form, transposed form
   - This task need not to take part in the final report.

2. FFT/IFFT
   - Develop instruction set extensions for Tensilica processor (TIE)
   - Use Fusion, SIMD, FLIX, knowledge from task 1
   - Compare DIT, DIF
   - Main task for the report and valuation.
Seminars

- Today, 10\textsuperscript{th} Oct., 4.DS, BAR/213/H:
  - Introduction to Lab
  - First information on Tensilica Instruction Set Extension
  - Demo on Xtensa Xplorer

- Tuesday, 7\textsuperscript{th} Nov., 4.DS, BAR/213/H:
  - Accounts ready to pick-up
  - Discussion/Solution to first task
  - Introduction to second task

- Further questions at any time during semester:
  - Make appointment via e-mail
  - If desired, discussion/consultation some weeks before the end of lab
Submission

Hand in via E-mail until 31st of March 2018

Grading:
- Archive with Tensilica workspace including optimized source code
- Project report in English (max. 3 pages w/o source code excerpts)

Assessment criteria:
- 50% practical work, 50% report

(Anonymous) publication of the results via Internet:
- Therefor necessary: your compliance with your signature
- Signature is voluntary!
- There will be no disadvantage for you, if you disagree with the publication!
- If you wish, your name can also be included in the publication
OVERVIEW
Benefits from this Lab

- Practical application of HW/SW Co-Design
- Get familiar with the Tensilica tool flow which is used by many companies today to create customized DSPs
- Grade for 0/0/2 course
Lab Approach

- RISC
- Enhanced RISC (ASIP)

Software

Compiler

Accelerate (by creating new instructions)

Your Task!
HW architecture: Xtensa LX5
Tensilica Tool Flow

Not part of the lab
RISC Pipeline

IF → ID → EX → M → WB

Extended Functional Accelerator Units

DMEM0
DMEM1

128-bit interface for SIMD

4x 32-bit integers

64 bit VLIW
Example: Bitmap Logical Operation Instruction
Creating New Instructions

Pure C code:

```c
short a, b;
int z1, z2;
z1 = a*b;
z2 = z1 >> 16;
```

TIE code:

```c
operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}
{
    wire [31:0] m = TIEmul(a[15:0], b[15:0], 1);
    assign z = {16'b0, m[31:16]};
}
```

C code with new instructions:

```c
#include <xtensa/tie/tie.h>
short a, b;
int z;
z = MUL_SRL_16(a, b);
```
Creating Pipelined Instructions

operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}
{
    wire [31:0] m = TIEmul(a[15:0], b[15:0], 1);
    assign z = {16'b0, m[31:16]};
}

schedule ms {MUL_SRL_16}
{
    use a 1;
    use b 1;
    def z 2;
}
operation MUL_SRL_16 {out AR z, in AR a, in AR b} {}
{
    wire [31:0] m1 = TIEmul(a[31:16], b[31:16], 1);
    wire [31:0] m0 = TIEmul(a[15:0], b[15:0], 1);
    assign z = {m1[31:16], m0[31:16]};
}
LOGIN PROCEDURE
Log in to remote computer with web browser

https://entmrدوا.ifn.et.tu-dresden.de/RDWeb
You will be asked for your credentials. Enter ifn\username and your password from the account information. After you logged in the first time, you will be requested to change your password.
Once logged in, click on RDS-lab
An `.rdp` file will be downloaded which opens a connection via Remote Desktop Protocol (RDP) to a Windows computer. Your operating system has to provide an RDP client.

- Click the Xplorer icon on the desktop to start Xtensa Xplorer.

**Hint:**

- Windows automatically provides the RDP client
- For Linux or Mac users, install an RDP client suitable for your operating system

If you cannot log in anyway, work at PC pool in FAL 250.
Build, run, profile and debug the complete C code

Select compile and optimization options:
Right click → “Build Properties”

Attach TIE file to coreLX5_hwsdcd:
Right click → “Attach TIE…”

Compile only TIE code:
Right click into TIE code window → “Compile TIE”

TIE area report
Xtensa Xplorer: TIE area report
Xtensa Xploror: Benchmark Perspective

- Total number of cycles per function
- Total number of cycles per instruction
- Total number of cycles per code line
- Processor pipeline to identify hazards
Xtensa Xplorer: Debug Perspective

- **Watch C variables and TIE wires**
- **Debug control**
- **Set breakpoints**
- **Watch memory content**
Export Xtensa workspace: Right click → “Export”

Export as “Xtensa Xplorer Workspace”
Browse and save the *.xws file to your local hard drive. Usually “C on your_PC_name”
Select your desired project
Do **not** export any
- Launches
- Configurations
- Tools
- Builds
- User-defined formats

but **do** export your TIE file(s)
Summary ➔ Click on “Finish”
TASK 1: FIR FILTER
Task 1: FIR Filter

- **FIR filter:**
  \[ y_n = \sum_{i=0}^{N-1} b_i x_{n-i} \]

- **Hot-Spots**
  - Multiply/Accumulate Operation (MAC)
  - Load input values/coefficients
  - Store output values

- **Different approaches:**
  1) Performing MAC on one input element with one coefficient
  2) Performing MAC on multiple elements in parallel \(\Rightarrow\) SIMD
  3) Separated instructions for Load, MAC and Store

```c
void fir_C(short *in, int *out, int len) {
    int n, i;
    for (n = 0; n < len+7; n++) {
        for (i = 0; i < 8; i++)
            out[n] += in[n+7-i]*coeff[i];
    }
}
```
SUMMARY
Summary

Your next TODOs:

- Register on list coming around
- Confirm your account
  - Pick up your account information at next introduction seminar or come to FAL 236
- Join next introduction session on 7th November
Contact & Rooms

Contact for Questions:
Sebastian Haas
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Room: FAL 236
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Room FAL 231

Website:
http://www.vodafone-chair.com
→ Teaching → Courses → „Praktikum HW/SW Co-Design”
http://mns.ifn.et.tu-dresden.de/Teaching/Courses/Pages/P-HWSW-Codesign.aspx

Questions?

Rooms
Admins: FAL 241
PC-Pool: FAL 250