Lecture "‘HW-SW Codesign’"

Solutions to Exercise (1)

1. (a) hint: include in your cut-set always all inputs (or outputs). This ensures that all output experience the same latency
   ⇒ total latency is 6

(b) latency is 2, but c.p. is longer
2. 4-bit carry-ripple adder

(a) signal flow graph for 4-bit adder

(b) The number of pipeline register is 21. For arbitrary bit-width $N$ we can write

$$n_p = \sum_{i=0}^{N-2} 2N - i = \frac{3N^2 - N - 2}{2} \quad (1)$$

(c) Adder row:
The skewing triangle is only necessary at the beginning and at the end, total latency is increased by one clock cycle per adder stage only

$\Rightarrow$ total latency and number of pipe-_registers reduced
3. Compare-Select circuit: Bit-level representation

(a) Subtraction and than selection according to sign bit

⇒ Loop at bit-level - c.p. can’t be shortened

(b) Bit-level comparison from MSB down to LSB

⇒ Cut-set similar to integrator - c.p. independent of width